UNIVERSITY OF MINES AND TECHNOLOGY, TARKWA

SECOND SEMESTER EXAMINATIONS, MAY 2018

COURSE NO: **CE 376**
COURSE NAME: **DIGITAL HARDWARE DESIGN**
CLASS: **CE 376** TIME: **3 HOURS**

Name**:** _____Index Number: _____

SECTION A

1. In digital electronics the semiconductor devices are classified into
   a. Unipolar
   b. Bipolar
   c. None of the above
   d. Bipolar and unipolar
2. The Schottky TTL are replace the TTL logic because of
   a. Fan out
   b. Fan in
   c. Power Dissipation
   d. Time Delays
3. ---------- complement is used for performing the BCD subtraction
   a. 6's
   b. 7's
   c. 8's
   d. 9's
4. What is the difference between digital and analog techniques?
   a. Digital quantities can take on any value over a continuous range.
   b. Digital quantities can take on discrete value over a range.
   c. Actually, they are indifferent, only digital is a new technology invented in 1980s.
   d. None of the above.
5. The most commonly used devices for fabricating the VLSI are ---------- devices.
   a. NMOS
   b. PMOS
   c. HMOS
   d. CMOS
6. All can be used to describe logic functions except?
   a. Algebraic expressions
   b. Truth -Table
   c. Hardware Description Language
   d. Description Language
7. Which logic IC is used for industrial applications

a. ECL
b. TTL
c. HTL
d. RTL

8. Which is/are called universal gates
   a. OR, AND gates
   b. NAND, NOR gates
   c. XNOR gate
   d. XOR gate
9. Which following is not an advantage of digital technique?
   a. Digital system is easier to design.
   b. Accuracy and precision are greater.
   c. Digital circuits are less affected by noise.
   d. Digital quantities are equivalent to real-world physical quantities.
10. An inverter
   a. performs the NOT operation
   b. changes a HIGH to a LOW
   c. changes a LOW to a HIGH
   d. changes a HIGH to a LOW
11. An AND gate gets a low output when
   a. no inputs are HIGH
   b. all inputs are HIGH
   c. any input is LOW
   d. Both A and C
12. Which of the following stores digital information?
   a. Combinational circuits
   b. Flip-flops
   c. DL logic family
   d. Both A and B
13. VHDL is a
   a. logic device
   b. PLD programming language
   c. computer language
   d. very high-density logic
14. An LSI device has a circuit complexity from
   a. 10 to 100 equivalent gates
   b. more than 100 to 10,000 equivalent gates
   c. 2000 to 5000 equivalent gates
   d. more than 10,000 to 100,000 equivalent gates
15. Which of the following is an SPLD?
   a. CPLD
   b. LCA
   c. PAL
   d. LAG
16. Which one of the following statements is correct?
   a. The architecture of CPLD is virtually the same as that of FPGA

b. Complexity of logic function is more in FPGA than CPLD

c. In system performance of FPGA is fast than CPLD

d. FPGA has limited programmability whereas CPLD has relatively unlimited programmability

17. Saturated logic circuits have inherently

a. short saturation delay time

b. low switching speed

c. higher power dissipation

d. lower noise immunity

18. The noise margin of a logic family is expressed in

a. decibel

b. watts

c. volts

d. none of the above

19. The main advantage of Schottly TTL logic family is its less

a. power dissipation

b. propagation delay

c. fan-in

d. noise-immunity

20. The fan-in of a logic gate refers to the number of

a. input devices that can be connected

b. input terminals

c. output terminals

d. circuits that can be connected at the output

21. The AND operation can be produced with

a. two NAND gates

b. three NAND gates

c. one NOR gate

d. three NOR gates

22. The OR operation can be produced with

a. two NOR gates

b. three NAND gates

c. four NAND gates

d. both A & B

23. The term bit means

a. a small amount of data

b. a binary digit

c. a 1 or a 0

d. both answers A and C

24. The Boolean algebra is essentially based on

a. symbols

b. algebraic laws

c. logic

d. truths

25. Different variables used in Boolean algebra can have values of

a. 0 or 1

b. LOW or HIGH

c. true or false

d. ON or OFF

26. In Boolean algebraic, ($A + AB$) referred to as the *Absorbtive* law outputs

a. A^2B
c. B
b. AB
d. A

27. When we De Morganise AB, we get

a. $\overline{AB}$
c. $\overline{A + B}$
b. $\overline{A} + \overline{B}$
d. $A + B$

28. The expression ABC can be simplified to

a. $\bar{A}B\bar{C}$
c. $A + \bar{A}B = A + B$
b. $AB + BC + CA$
d. $\overline{A} + \overline{B} + \bar{C}$

29. Which of the following Boolean algebra rules is correct?

a. $A\bar{A} = 1$
c. $A + \bar{A}B = A + B$
b. $A + AB = A + B$
d. $A\,(A + B) = B$

30. Simplified form of Boolean expression ($A + \overline{B} + \bar{A}B$) C is

a. 1
c. C
b. 0
d. $\bar{C}$

31. What is the largest decimal number that can be represented using 8 bits?

a. 128
c. 256
b. 255
d. 1024

32. Subtractor are designed by using which of the following ICs?

a. Adder
c. Multiplier
b. Subtractor
d. All the above

33. To get an output of 1 (high) from a circuit in which the output of an OR gate is one of the input terminals of an AND gate, the inputs will either have the combination

a. 001
c. 011
b. 110
d. 000

Fill in the Blanks

34. The temperature range in which an IC functions for military applications --------- whereas that of industrial applications is ---------

35. When the logic blocks are relatively simple, the FPGA architecture is called ---------

36. Minimum voltage available at output corresponding to logic 1 is called ---------

37. ---------- is the voltage difference between the guaranteed output voltage level and the required input voltage level of a logic gate.

38. --------- is the time required for a change in logic level to travel from the input to the output of a logic gate.
39. The --------- has programmable AND gate array and fixed OR array whereas the --------- does the same thing but is configurable multiple times?
40. The ---------- is a measure of how fast the logic system can operate and it's indicated by the ---------- point on the pulse edge.

SECTION B

Attempt any three of the questions below

1. Define the following acronyms: CPLD, FPGA, HDL, VHDL, CMOS, LSI, SMT, PCB,
2. Draw a digital circuit consisting of 2-input AND gates and three inverters where an inverter is connected to each of the AND gate's inputs and its output. For each of the four possible combinations of inputs connected to the two primary inputs of this circuit, determine the value produced at the primary output.
3. Design a BCD-to-Excess-3 code converter circuit. Produce the following:
    a. Truth table of design specifications;
    b. Logic function expressions for your design;
    c. Circuit diagram
4. Design a 4-bit Carry Look-Ahead Adder circuit. Produce the following:
    a. Truth table of design specifications;
    b. Logic function expressions for your design;
    c. Circuit diagram

Examiners: Fatao