UNIVERSITY OF MINES AND TECHNOLOGY, TARKWA

SECOND SEMESTER EXAMINATIONS, MAY 2018

COURSE NO: CE 278

COURSE NAME: **EMBEDDED SYSTEMS**

CLASS: TIME: 3 HRS

Name**:** _____Index Number: _____

Answer all questions in sections A and B and any one question in the section C

Section A (each question answered correctly is 1 mark)

1. Which of the following is/ are example(s) of embedded system for signal processing?
   a. Apple IPod
   b. In-the-canal hearing Aid
   c. SanDisk USB Mass storage device
   d. None of the above
2. Little Endian Processors
   a. Stores the lower-order byte of data at the lowest address and the high-order byte of data at the at the highest address of memory
   b. Stores the high-order byte of data at the lowest address and the lower-byte of data at the lowest address of the memory.
   c. Stores both high order and low order byte of data at the same address
   d. None of these
3. The instruction set of CISC processor
   a. Simple and lesser in number
   b. Complex and lesser in number
   c. Simple and larger in number
   d. Complex and larger in number
4. Which of the following processor architecture supports easier instruction pipelining?
   a. Harvard
   b. Von-Neumann
   c. Both of them
   d. None of them
5. Which of the following is a one-time programmable memory?
   a. SRAM
   b. PROM
   c. FLASH
   d. NVRAM
6. Which of the following is an example of input sub-system of embedded system dealing with digital data?
   a. Analog to Digital Converter
   b. Optocoupler
   c. Digital to Analog Converter
   d. All of the above
7. Which of the following is true about the Princeton Architecture

a. Has a separate bus for instruction fetching and data fetching
b. Implementation is relatively at a high cost
c. It is easier for pipelining
d. None of the above

8. Application code instructions when loaded onto the embedded system could be stored in the
   a. Static RAM
   b. Non-Volatile RAM
   c. Dynamic RAM
   d. None of the above
9. In order for a 7 segment LED display to display the numerical value 5 which of the segments would be set
   a. AFDGE
   b. AFGCD
   c. DGABF
   d. DGFEC
10. Which of the following is not an I/O sub-system of embedded system
    a. Light Emitting Diode
    b. 7 segment LED display
    c. Electromechanical replay device
    d. Matrix keyboard
    e. All the above
11. The on board communication interface of microprocessor/ controller embedded system applications includes
    a. Serial Peripheral Interface (SPI)
    b. I-Wire
    c. Universal Asynchronous Receiver/Transmitter (UART)
    d. All the Above
    e. None of the above
12. The processor /CPU includes the processor core (CPU core) surrounded by lots of supportive processor specific peripherals. If the process core acts as the basic computation engine of the processor, which of the following is not true about the processor core
    a. Has its own register sets
    b. Pipeline engine to boost instruction execution
    c. Instruction decoder to decode instruction fetched from the program memory
    d. All the above
    e. Only (a) and (c)
13. The ARM Cortex Mx processor core has two operating modes namely
    a. Privilege access level mode
    b. Handler Mode
    c. User mode
    d. All the above

e. (b) and (c)

14. Ideally the processor core begins execution with the ……" and whenever an interrupt/ exception is encountered then it switches to the …… in order to service the ISR associated with that system exception or interrupt.

a. Thread Mode, User Mode
b. Handler Mode, User Mode
c. User mode, Handler Mode
d. Handler Mode, Thread Mode

15. The ARM Cortex Mx offer two access levels namely the Privilege Access Level (PAL) and Non-Privilege Access Level (NPAL). Which of the following statement(s) is/are true:

(I) By default embedded system application codes run in the user mode and PAL;

(II) The handler mode code execution is always in the NPAL;

(III) Thread mode can only operate in the NPAL; and

(IV) It is possible for the processer core to switch between the NPAL and PAL by setting or resetting the bit [1] of the control register.

a. I only
b. I and III
c. II, IV and I
d. IV only

16. The Special purpose registers of the ARM cortex M core processor include

I. Application Program status registers
II. Program Counter
III. FAULT MASK registers
IV. Interrupt Program status registers
V. Main Stack Pointer
V. Link Register

a. III, II, and IV
b. V, IV, III
c. III, V and IV
d. I, III, and IV

17. The Exception mask registers, Program Status Registers and Control registers are…….. in size.

a. 16-bytes
b. 32-bits
c. 32 bytes
d. 16-bits

18. The Exception Mask Register as part of the special purpose registers of the ARM processor does not include

a. Priority Mask Register
b. Base Priority Mask Register
c. Interrupt Mask Register
d. Fault Mask Register

19. Which of the statement(s) is/are false about the Priority Mask Register and Fault Mask Registers;

    I. The Priority Mask Register when reset prevents activation of all exceptions with programmable priority; and it is only accessible in privileged access level mode.

    II. The Fault Mask Register when set prevents activation of all exceptions except for the Non-Maskable Interrupt (NMI); and it is only accessible in privileged access level mode.

    III. The Fault Mask Register when reset prevents activation of all exceptions with programmable priority; and it is only accessible in privileged access level mode.

    IV. The Priority Mask Register when set prevents activation of all exceptions with programmable priority; and it is only accessible in privileged access level mode.

    a. III and II
    c. II and IV
    b. I and III
    d. I only

20. Which of the following is not part of the memory map of the ARM cortex M Processor?

    a. Code Region
    c. SRAM Region
    b. Peripheral Region
    d. Application Specific region

21. Which of the memory regions of the ARM Cortex M processor supports bit banding?

    a. Static RAM and External RAM regions
    c. Static RAM and Peripherals Regions
    b. Internal and External Peripheral Bus regions and Peripherals regions
    d. Code and Static RAM regions

22. Which of the memory regions of the ARM Cortex can application code not be executed from?

    a. Code Regions
    c. Static RAM region
    b. Peripheral Regions
    d. External RAM region

23. What is the value of the bit-band alias address to the 6^{th} bit of the SRAM code region address 0x200000004.

    a. 0x22000152
    c. 0x22000146
    b. 0x22000088
    d. 0x22000098

24. What is the value of the bit-band alias address to the 6^{th} bit of the SRAM code region address 0x200000012

    a. 0x22000258
    c. Ox22000158
    b. Ox22000298
    d. 0x22000198

25. The ARM Cortex Mx offer two access levels namely the Privilege Access Level (PAL) and Non-Privilege Access Level (NPAL). Which of the following statement(s) is/are false:

I. By default embedded system application codes run in the user mode and PAL;

II. The handler mode code execution is always in the NPAL;

III. Thread mode can only operate in the NPAL; and

IV. It is possible for the processer core to switch between the NPAL and PAL by setting or resetting the first bit of the control register.

a. I and IV
c. III and II
b. IV and II
d. I and III

Section B (each question answered correctly is 1 mark)

1. Microprocessors/ controllers based on the Harvard architecture will have separate data bus and instruction bus. This allows the transfer of data and program fetching to occur simultaneously on both buses. (True/ False)

2. EEPROM memory is alterable at the byte level. (True/ False)

3. Execution of program from ROM is faster than the execution from RAM. (True/ False)

4. The Static RAM stores data in the form of charges and the Dynamic RAM stores data in the form of voltage. (True/ False)

5. During code execution when the processor receives an interrupt from any peripheral, it would switch from the "handler mode" to the "thread mode" associated with the interrupt service routine of the exception or interrupt. (True/ False)

6. If the application code of the embedded system designer switch the processor from the Privilege Access Level (PAL) to Non Privilege Access Level (NPAL) using the control register, would it be possible switch back to the PAL whilst in the user mode? (True/ False)

7. A register is one of a small set of storage places that are part of the computer processor core. It can hold (a) Operands (b) Opcodes and (c) storage addresses. (True/ False)

8. All the following registers can be accessed by the processor core using Privilege Access Level (I) Interrupt Program Status register (II) Application Program Status Register (3) NVIC registers (IV) Control Register (V) Main Stack Pointer. (True/ False)

9. The Priority Mask Register when reset prevents activation of all exceptions with programmable priority; and it is only accessible in privileged access level mode. (True/ False)

10. The Fault Mask Register when set prevents activation of all exceptions except for the Non-Maskable Interrupt (NMI); and it is only accessible in privileged access level mode. (True/ False)

11. Name the two configuration modes of the 7 segment LED display namely the ……. and …….

12. The push button Input sub-system comes in two configuration mode namely ……and ……..

13. The Program status registers holds the status of the current execution of the program. It consist of three registers. Name any two. ;……(1)…….and ……..(2)……..

14. What is the value of the bit-band alias address to the 24th bit of the SRAM code region address 0x400000012. Ans:…….

15. What is the value of the bit-band alias address to the 24th bit of the SRAM code region address 0x40000008. Ans:……..

16. Assume R3 equals 0x2000.0000 and R4 equals 0x2000.0016 at the time LDR R2,[R3,R4] is executed. What address will be accessed?

17. An exception refers to events that emanates asynchronously either from an external world or from the internal system. What are the 2 types of exception of the ARM Cortex Mx processor? Ans:……(1)…… and ……(2)……..……

18. The ARM Cortex Mx has 15 system exceptions. Which of the 15 systems exceptions has fixed priority? Ans:……..

19. When the priority grouping of a 3bit implementable priority level register is 5, how many pre-empt priority levels do exist. Ans: ……..

20. Within the ARM Cortex M processor, there exist a number of registers which are programmable for managing interrupts. They are the NVIC registers. Mention any two of the NVIC registers. Ans: …….

Section C (A question answered correctly is 15 mark)

Question 1

(a): When priority group =7 for a 3-bit implementable priority level register of an ARM Cortex processor find out

i. Pre-empt priority width (1 mark)
ii. Pre-empt priority programmable levels (1 mark)
iii. Implementable Pre-empt priority Programmable levels (1 mark)
iv. Sub-priority width (1 mark)
v. Sub-priority programmable levels (1 mark)
vi. Implementable Sub-priority Programmable level (1 mark)
vii. Give a conclusion (1 mark)

(b): Briefly explain the usage of the pre-empt priority field and sub-priority fields of the priority level registers (2 marks).

(c): Mention any of two of the addressing modes of the ARM assembly language (2 marks)

(d): Mention any two of the NVIC registers (1 mark)

(e): What is Direct Memory Access (DMA)? (3 marks)

Question 2

(a): Briefly explain how an interrupt generated? (2.5 marks)

(b): Briefly describe the five sequences which take place after an interrupt is generated after which the interrupt service routine is executed. (2.5 marks)

(c): Assume R3 equals 0x2000.0000 and R4 equals 0x2000.0016 at the time LDR R2, [R3,R4,LSL#2] is executed. What address will be accessed? (2 marks)

(d): Write an assembly language Program which sums up multiples of 8 five times using an ARM Cortex M3 processor core. (5 marks)

(e): Briefly describe bus arbitration. (3 mark)