UNIVERSITY OF MINES AND TECHNOLOGY, TARKWA

FIRST SEMESTER EXAMINATIONS, NOV/DEC 2018

COURSE NO: CE 271
COURSE NAME: MICROPROCESSORS AND MICROCONTROLLERS
CLASS: CE II **TIME:** 2 HOURS

Name**:** _____Index Number: _____

INSTRUCTIONS: *Attempt **ALL QUESTIONS** in **SECTIONS A** and **SECTION B***

SECTION A: *Answer All Questions on the question paper by circling or ticking (√) the correct answers.*

1. A 32-bit processor has _____.
   a) 32 registers.
   b) 32 I/O devices.
   c) 32 Mb of RAM.
   d) 32-bit registers.
2. Pipelining improves CPU performance due to _____.
   a) Reduced memory access time.
   b) Increase clock speed.
   c) The introduction of parallelism.
   d) Additional functional units.
3. A 32-bit address bus approximately allows access to a memory of capacity of _____.
   a) 64 Mb.
   b) 16 Mb.
   c) 1 Gb.
   d) 4 Gb.
4. Given that the subprogram PUTC displays a character in the AL register, the effect of the following instruction:

   MOV AL, 'C';
   SUB AL, 2;
   CALL PUTC;

   a) Is to display 2.
   b) Is to display 'C'.
   c) Is to display 'a'.
   d) Is to display a blank.
5. Which of the following is an illegal instruction?
   a) OR bx, bx;
   b) INC AL, 1;
   c) ADD ax, 30;
   d) MOV ax, 30000;
6. To copy the hexadecimal number A to the BH register you write _____.

a) MOV 0bh, ah;
c) MOV bh, ah;
b) MOV bh, 0a;
d) MOV bh, [ah];

7. The effect of the following instructions below:

MOV ah, 2h;
INT 21h;
is to
a) Read a character into AL.
c) Display the character in AL.
b) Read a character into DL.
d) Display the character in DL.

8. The effect of the following instructions below:

MOV ah, 1h;
INT 21h;
is to _____.
a) Read a character into AL.
c) Display the character in AL.
b) Read a character into DL.
d) Display the character in DL.

9. The instruction MOV str [SI], 'a'; is an example of _____.
a) Indirect addressing.
c) Direct addressing.
b) Indexed addressing.
d) Register addressing.

10. The instruction JE label is an example of _____.
a) Indirect addressing.
c) Relative addressing.
b) Indexed addressing.
d) Immediate addressing.

11. Which of the following is an illegal 8085 instruction _____?
a) HLT 2;
c) AND B, 300;
b) PUSH B;
d) MOV B, A;

12. The BP register is typically used for accessing _____.
a) Strings.
c) Stack.
b) Memory.
d) Data segment.

13. The RET instruction modifies the _____.
a) Instruction registers.
b) Program counter.

c) Address register.
d) Flag register.

14. The SP register is typically used for accessing _____.

a) Strings.
c) Stack.
b) Memory.
d) Data register.

15. The decimal number 127 may be represented by _____.

a) 1111 1111b
c) EEh
b) 1000 0000b
d) 0111 1111b

16. The maximum number of bits required to store the hexadecimal number FF is _____.

a) 2.
b) 4.
c) 8.
d) 16.

17. Cache memory enhances _____.

a) Memory capacity.
c) Secondary storage capacity.
b) Memory access time.
d) Secondary storage access time.

18. Which of the following is NOT a type of processor?

a) Motorola 8086.
c) Motorola 6800.
b) Intel Pentium.
d) Z80.

19. IBM PC's were originally based on the _____.

a) Intel 80x86 processor family.
c) Z80 family.
b) Motorola 6800 family.
d) Power PC family.

20. A GUI is _____.

a) Hardware.
c) Software interface.
b) Language interpreter.
d) An operating system.

21. A virtual memory is _____.

a) Related to virtual reality.
c) A form of RAM.
b) A form of ROM.
d) A form of flash memory.

22. Timesharing is the same as _____.

a) Multitasking.
c) Multiuser.
b) Multiprogramming.
d) Multicasting.

23. A compiler _____.

a) A fast interpreter.
b) Slower than an interpreter.
c) Converts a program to machine code.
d) Assembles a program.

24. "ZIPPING" a file means _____.

a) Encrypting it.
b) Decrypting it.
c) Compressing it.
d) Transmitting it.

25. An assembly language instruction _____.

a) Always has a label.
b) Always takes at least 1 operand.
c) Always has an operation field.
d) Always modifies the status register.

26. A data movement instruction will _____.

a) Modify the status register.
b) Modify the stack pointer.
c) Modify the program counter.
d) Transfer data from one location to another.

27. The memory address register is used to store _____.

a) Data to be transferred to or from memory.
b) Data to be transferred to the stack.
c) The address of a memory location.
d) An instruction that has been transferred from memory

28. CISC machines _____.

a) Have fewer instructions than RISC machines.
b) Use more RAM than RISC machines.
c) Have medium clock speeds.
d) Use variable size instructions.

29. CPU performance may be measured in _____.

a) BPS. b) MIPS. c) MHz d) VLSI.

30. The IBM/Motorola PowerPC 601 processor is _____ bits?

a) 16. b) 32. c) 64. d) 8.

31. The Motorola 68000 processor is _____ bits?

a) 16. b) 32. c) 64. d) 8.

32. Which of the following is an illegal 8086 instruction?

a) MOV 20, bx;
b) INC AL;
c) AND bx, bx;
d) ADD ax, 30;

33. Which of the following variables uses the most amount of RAM.

a) X db 255;
b) Y db 80 dup ('Z');
c) Z dw 50 dup (0);
d) Small dd 40 dup (0);

34. Which of the following is NOT a MASM directive?

a) . STACK
b) DB
c) . MODEL
d) C

35. Programs are written in assembly language because they _____.

a) Run faster than HLL programs.
b) Are portable.
c) Easier to write than machine code programs
d) They allow the programmer access to registers or instructions that are not usually provided by an HLL.

36. The instruction INC I where I is a memory variable involves _____.

a) A memory read operation.
b) A memory write operation.
c) A memory read and a memory write operation.
d) Only an arithmetic operation.

37. The program counter _____.

a) Stores the address of the instruction that is currently being executed.
b) Stores the next instruction to be executed.
c) Stores the address of the next instruction to be executed.
d) Stores the instruction that is being currently executed.

38. In the 8086 processor, an example of a non-maskable interrupt is _____.

a) Trap. b) RST 6.5. c) INTR. d) RST 7.5.

39. What is the output of the following code:

PUSH AL;

a) Decrement SP by 2 & push a word to stack.

b) Increment SP by 2 & push a word to stack.

c) Decrement SP by 2 & push a word to stack.

d) Illegal.

40. What is the output of the following code:

AX=3707h, BH=151 decimal.

DIV BH;

a) AL= 65H, AH=94 decimal.

b) AL=5EH, AH=101 decimal.

c) AH=E5H, AL=5EH.

d) AL=56H, AH=5E

[20 MARKS]

SECTION B

Answer **All Questions** by providing the correct answers in the spaces made available.

1. In 8086, logical address is described by combining _____ and _____.
2. List all the interrupt inputs of the Intel 8086 microprocessor.

   _____

   _____

   _____

   _____

   _____
3. A/An _____ is a pointer to where the ISR is stored in memory.
4. The two (2) ways the keyboard is interfaced with the CPU is either

   _____ or _____
5. The three (3) basic multiprocessor configurations are?

   _____

   _____

   _____
6. Indicate by writing in the spaces provided if its legal/illegal Intel 8086 instruction.
   a. MOV AL, [BX]: _____

b. INC DI: _____

c. AND [BX], [SI]: _____

d. ADD [DI+2], [BX+CX]: _____

e. OUT 7, AX: _____

f. POP 23H: _____

g. SAL AL, 1: _____

h. CALL [B]: _____

i. DCR [BC]: _____

j. TEST AL, 10B: _____

7. List five (5) pins on the Intel 8085 microprocessor used for interfacing with other devices?

   _____

   _____

   _____

   _____

   _____

8. What is the effect of the following instruction **XOR CX, 240 h** if content of register CX is 125A h? _____

9. The CALL instruction modifies which registers in the Intel 8086?

   _____

10. The _____ register specifies the type of external interrupt to the Intel 8051 microcontroller.

11. The _____ interrupt has the highest priority on the Intel 8086 microprocessor?

12. List all the five (5) maskable interrupt signals on the Intel 8051 microcontroller?

    _____

    _____

    _____

    _____

    _____

13. Give three (3) architectural features of the Intel 8051 microcontroller?

_____

_____

_____

_____

_____

_____

14. Give examples of instructions using the following addressing modes on the Intel 8086 microprocessor?

a. Immediate Addressing mode: _____

b. Register Addressing Mode: _____

c. Index Addressing Mode: _____

d. Based-Index Addressing Mode: _____

e. Based-Index with Displacement: _____

15. The Intel 8086 Microprocessor is divided into two functional units which are?

_____

_____

[50 MARKS]

T. Kwantwi